ABSTRACT OF THE DISCLOSURE

When normal bit lines BL3 and /BL3 are selected, spare bit lines SBL2 and /SBL2 are simultaneously selected, so that column select gates are placed in such a manner that these bit line pairs are connected to respective different read data bus pairs. The column select gates are distributed in placement so as not to cause a great difference in load capacitance between read data buses. A redundancy determination result is reflected on read data by activation of control signals $\phi 1$ and $\phi 2$ given immediately prior to a sense amplifier. Note that two sense amplifier may be provided with control signals $\phi 1$ and $\phi 2$ so as to select the outputs of one sense amplifier. With such a configuration adopted, it is possible to provide a memory device capable of performing high speed reading while realizing a redundancy replacement.